REMARKS

By this amendment, claims 1 and 4 have been amended, and claims 9-16 have been added. Thus, claims 1-16 are now active in the application. Reexamination and reconsideration of the application is respectfully requested.

The specification has been carefully reviewed and revised to correct grammatical and idiomatic errors in order to aid the Examiner in further consideration of the application. The amendments to the specification are incorporated in the attached substitute specification. No new matter has been added.

In items 1-4 on pages 2-4 of the Office Action, claims 1-4 were rejected under 35 U.S.C. § 102(e) as being clearly anticipated by Ipposhi et al. (US 2003/0094674); and claims 5-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ipposhi et al. in view of Sze ("Semiconductor Devices-Physics and Technology"). These rejections are respectfully traversed, and it is respectfully submitted that these rejections are clearly inapplicable to the claims as currently presented, for the following reasons.

Claims 1-8 are directed to a wafer support plate 10 for supporting a semiconductor wafer W, and independent claim 1 specifically requires the wafer support plate 10 to comprise: a support surface 11 on which the semiconductor wafer W is to be supported; and a crystal orientation mark (e.g. 12, 22, 32) which indicates a crystal orientation of the supported semiconductor wafer W.

Claims 9-16 set forth a semiconductor wafer arrangement, and independent claim 9 specifically requires the arrangement to include: a semiconductor wafer W; and a wafer support plate 10 comprising a support surface 11 on which the semiconductor wafer W is supported, and a crystal orientation mark (e.g. 12, 22, 32) which indicates a crystal orientation of the supported semiconductor wafer W.

In contrast to the present invention of claims 1 and 9, the Ipposhi et al. reference (US 2003/0094674) in directed to a semiconductor wafer having, as its constituent elements, a wafer 1 for the support substrate, an SOI layer 3 and an oxide film layer 2 (see page 1, paragraphs [0004]-[0008]; and see page 4, paragraph [0060] of Ipposhi et al). Further, please see paragraphs [0054] and [0055] of the "Brief Description of the Drawings" which describe Figs. 17 and 18 as showing "the conventional semiconductor wafer". Thus, all of the elements, including the support substrate wafer 1, the oxide film

layer 2 and the SOI layer 3 of Ipposhi et al. **are constituent elements of the semiconductor wafer per se.** It is further specifically noted that, paragraph [0006] of Ipposhi et al. states: "a wafer 1 for the support substrate formed of a silicon substrate", which also indicates that the support substrate 1 of Ipposhi et al. is a constituent element of the overall semiconductor wafer.

On the other hand, each of the independent claims 1 and 9 requires the presence of a wafer support plate for supporting a semiconductor wafer, and this wafer support plate is not a constituent element of the semiconductor wafer, but is an element that is independent of the semiconductor wafer. The support plate 10 is used for supporting a semiconductor wafer W during machining, such as grinding or cutting of the semiconductor wafer, and the support plate is to be formed of glass, metal, ceramics or synthetic resin (as recited in claims 5-8 and 13-16).

Furthermore, in the present invention, the crystal orientation mark (e.g. 12, 22, 32) in the wafer support plate 10 is provided to supplement a crystal orientation mark provided on the semiconductor wafer W to be supported on this support plate 10, to guard against the occasion when the crystal orientation mark N of the semiconductor wafer W becomes unrecognizable due to chipping of the outer periphery of the semiconductor wafer during machining. Thus, if such chipping occurs during machining such that the crystal orientation mark of the semiconductor wafer becomes unrecognizable, the crystal orientation mark of the support plate will remain recognizable. The support plate 10 is an independent element relative to the semiconductor wafer W and is intended to be removed from the semiconductor wafer after machining to be reused for another semiconductor wafer.

In contrast, in the conventional arrangement shown in Figs. 17 and 18 of the Ipposhi et al. reference, a semiconductor wafer is provided that comprises a wafer layer 1 and a wafer layer 3 with a crystal orientation of the wafer layer 1 shifted from a crystal orientation of the wafer layer 3, by using the crystal orientation display sections or marks on the wafer layers 1 and 3. In other words, both of the orientation display marks 1a, 3a in Figs. 17 and 18 of Ipposhi et al. are provided on the semiconductor wafer per se and not on a support plate as is the case in the present invention. The crystal orientation

marks 1a, 3a in the Ipposhi et al. reference are formed for use in manufacturing the semiconductor wafer itself.

Thus, for the above reasons, it is believed apparent that the present invention as recited in claims 1 and 9 is not anticipated by the Ipposhi et al. reference. Furthermore, the differences as discussed above between the present invention of claims 1 and 9 and the Ipposhi et al. reference are such that a person having ordinary skill in the art would clearly not have been motivated to modify the Ipposhi et al. arrangement of constituent elements 1, 2 and 3 that constitute a semiconductor wafer, in such a manner as to result in or otherwise render obvious the present invention as recited in claims 1 and 9. Therefore, it is respectfully submitted that claims 1 and 9, as well as claims 2-8 and 10-16 which respectively depend therefrom, are clearly allowable over the prior art of record.

The Examiner cited the Sze article for disclosing the use of silicon dioxide as the oxide layer for an SOI substrate. However, this article provides no teaching or suggestion that would have obviated the above-discussed shortcomings of the Ipposhi et al. reference.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice thereof is earnestly solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, it is respectfully requested that the Examiner contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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